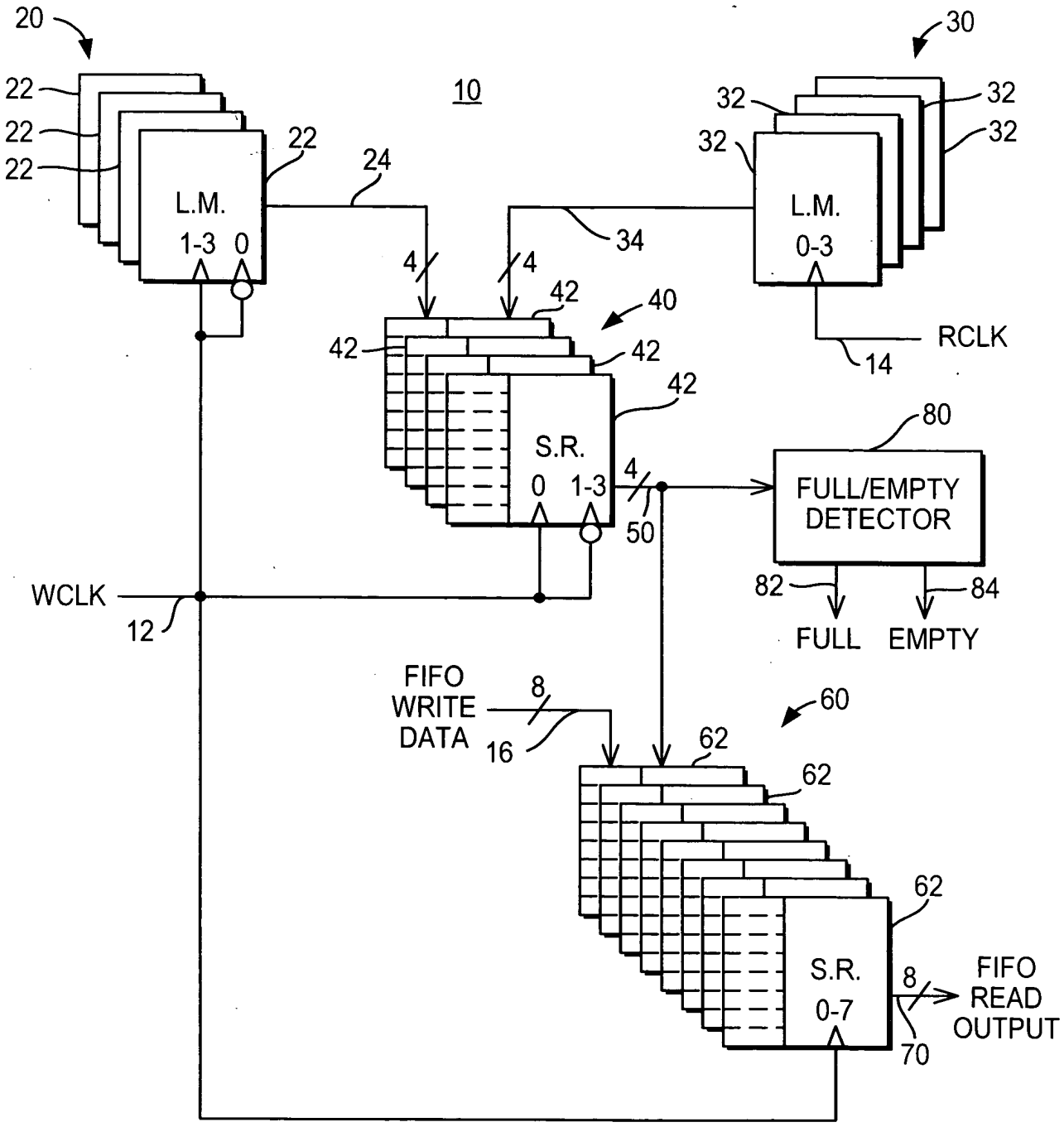

20
22
22
22
L.M.
1-3 0
22
24
10
30
32
32
32
32
L.M.
0-3
34
4
4
42
40
42
42
42
S.R.
0 1-3
4
50
RCLK
14
80
FULL/EMPTY
DETECTOR
82
84
FULL
EMPTY
WCLK
12
FIFO
WRITE
DATA
8
16
60
62
62
62
S.R.
0-7
8
70
FIFO
READ
OUTPUT

FIG. 1

GRAY CODE WORD				EQUIVALENT DECIMAL VALUE
D (MSB)	C	B	A (LSB)	
* 0	0	0	0	0
0	0	0	* 1	1
0	0	* 1	1	2
0	0	1	* 0	3
0	* 1	1	0	4
0	1	1	* 1	5
0	1	* 0	1	6
0	1	0	* 0	7
* 1	1	0	0	8
1	1	0	* 1	9
1	1	* 1	1	10
1	1	1	* 0	11
1	* 0	1	0	12
1	0	1	* 1	13
1	0	* 0	1	14
1	0	0	* 0	15

FIG. 2

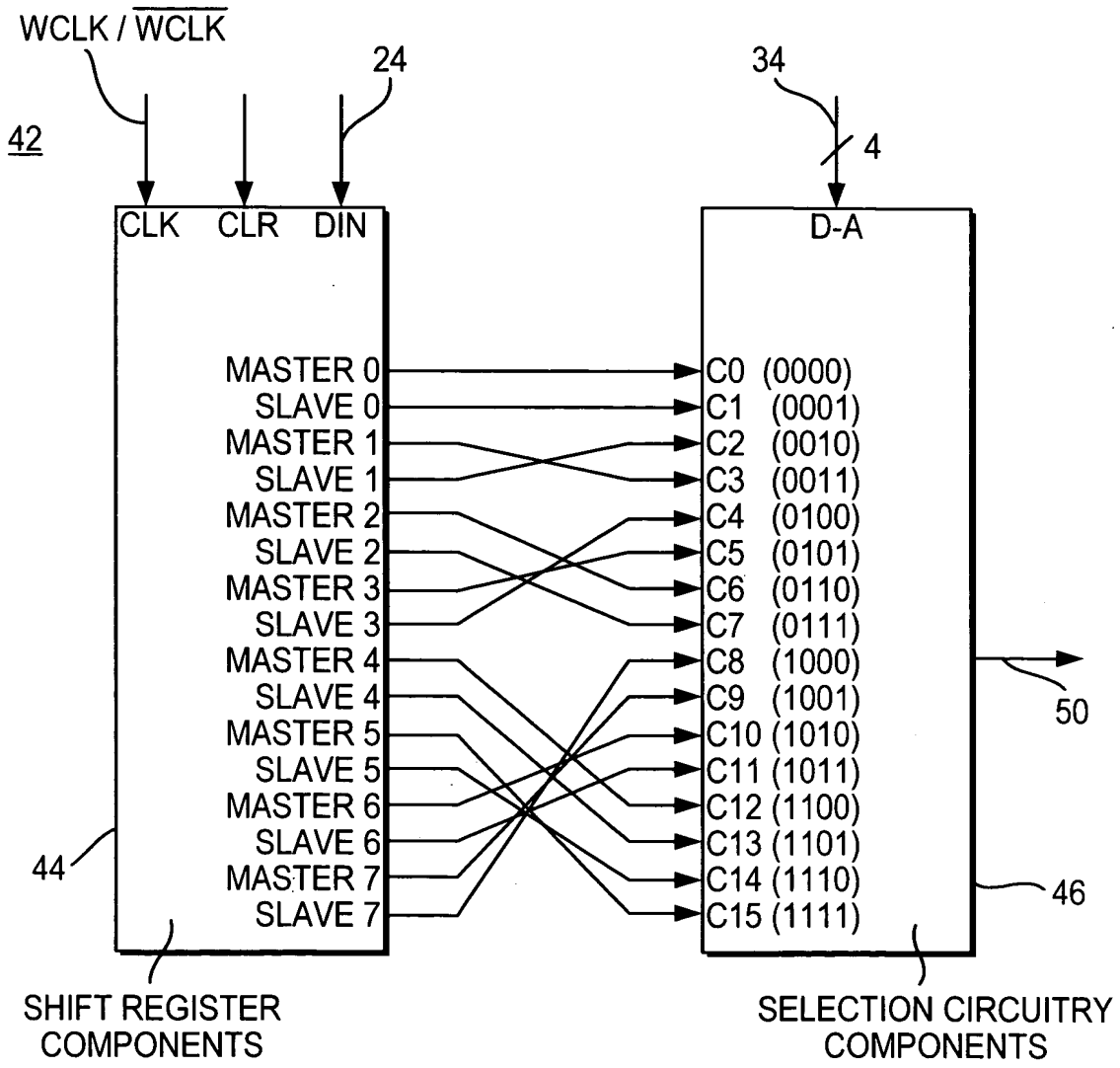

WCLK / $\overline{WCLK}$
24
34
42
4
CLK
CLR
DIN
D-A
MASTER 0
SLAVE 0
MASTER 1
SLAVE 1
MASTER 2
SLAVE 2
MASTER 3
SLAVE 3
MASTER 4
SLAVE 4
MASTER 5
SLAVE 5
MASTER 6
SLAVE 6
MASTER 7
SLAVE 7
C0 (0000)
C1 (0001)
C2 (0010)
C3 (0011)
C4 (0100)
C5 (0101)
C6 (0110)
C7 (0111)
C8 (1000)
C9 (1001)
C10 (1010)
C11 (1011)
C12 (1100)
C13 (1101)
C14 (1110)
C15 (1111)
50
44
46
SHIFT REGISTER COMPONENTS
SELECTION CIRCUITRY COMPONENTS

FIG. 3

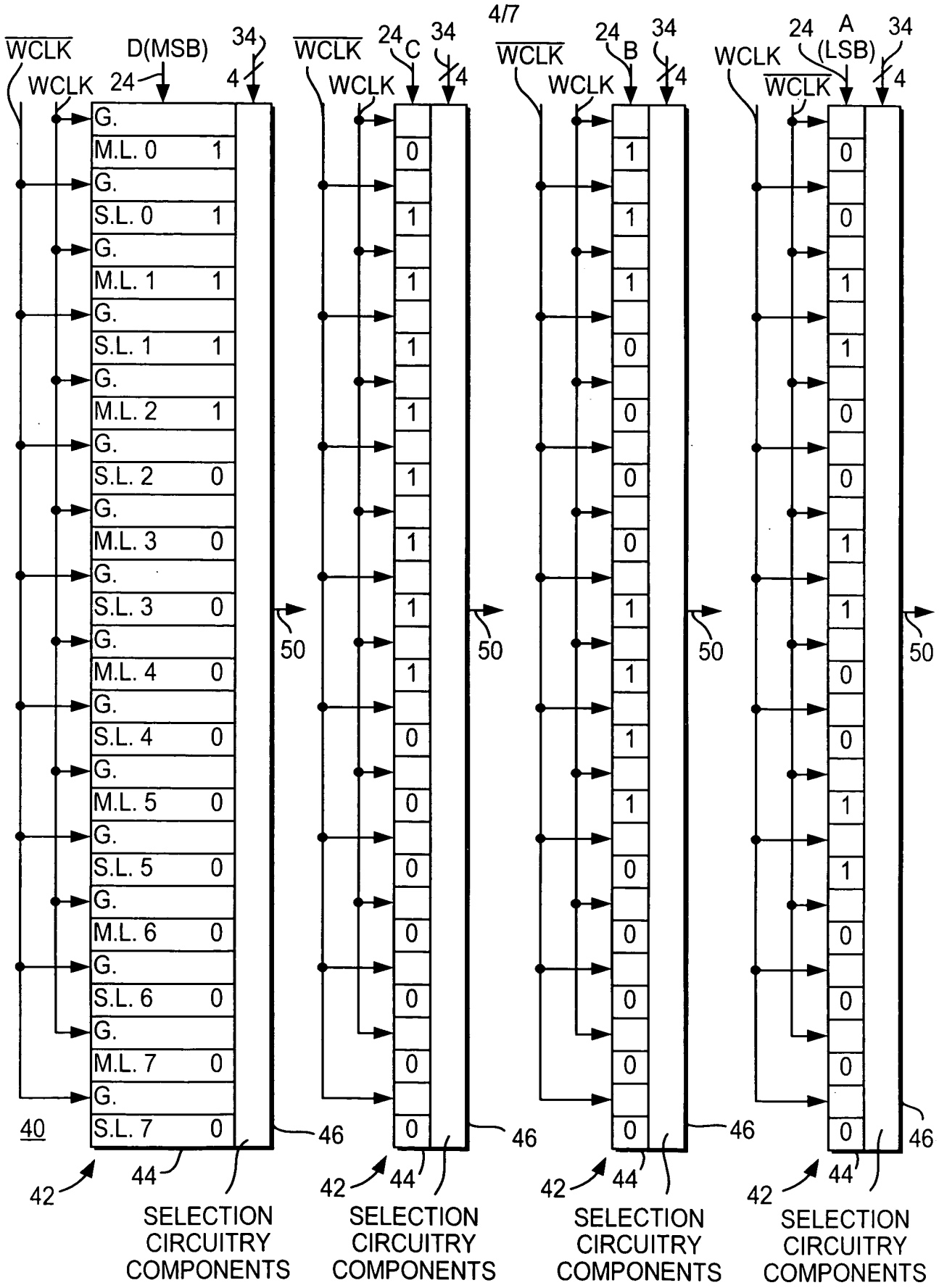

4/7
WCLK
D(MSB)
24
34
4
C
B
A
(LSB)
G.
M.L. 0 1
S.L. 0 1
M.L. 1 1
S.L. 1 1
M.L. 2 1
S.L. 2 0
M.L. 3 0
S.L. 3 0
M.L. 4 0
S.L. 4 0
M.L. 5 0
S.L. 5 0
M.L. 6 0
S.L. 6 0
M.L. 7 0
S.L. 7 0
40
42
44
46
50
SELECTION CIRCUITRY COMPONENTS

FIG. 4

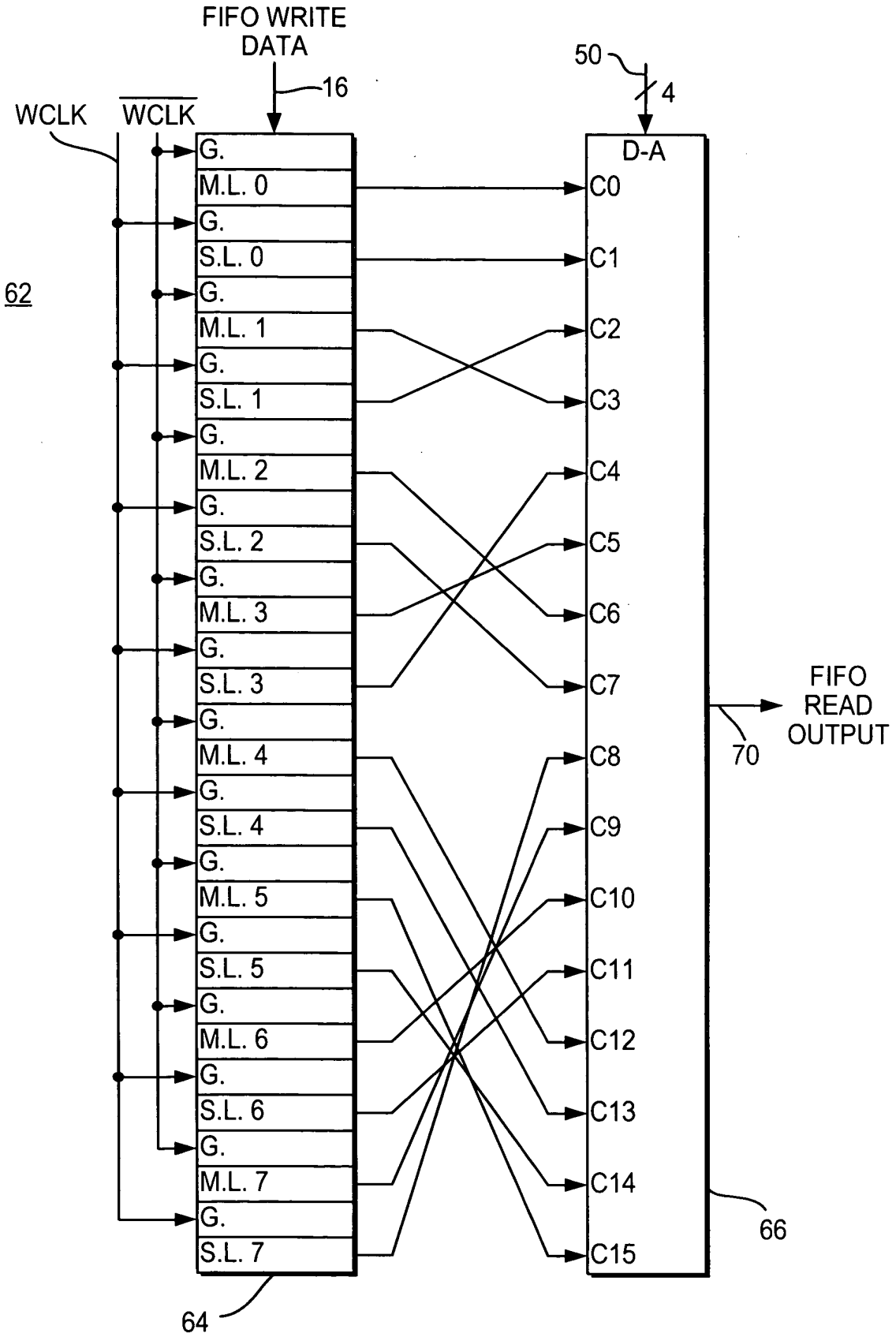
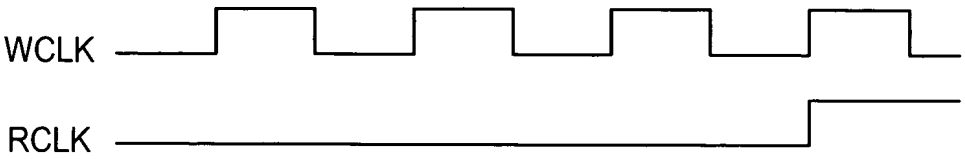

FIFO WRITE DATA
16
50
4
WCLK
WCLK
62
G.
M.L. 0
G.
S.L. 0
G.
M.L. 1
G.
S.L. 1
G.
M.L. 2
G.
S.L. 2
G.
M.L. 3
G.
S.L. 3
G.
M.L. 4
G.
S.L. 4
G.
M.L. 5
G.
S.L. 5
G.
M.L. 6
G.
S.L. 6
G.
M.L. 7
G.
S.L. 7
64
D-A
C0
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
66
FIFO READ OUTPUT
70

FIG. 5



MASTER 0	D0	D0	D1	D1	D2	D2	D3	D3	
SLAVE 0		D0	D0	D1	D1	D2	D2	D3	
MASTER 1			D0	D0	D1	D1	D2	D2	
SLAVE 1				D0	D0	D1	D1	D2	
MASTER 2					D0	D0	D1	D1	
SLAVE 2						D0	D0	D1	
MASTER 3							D0	D0	b
SLAVE 3								D0	a

FIG. 6

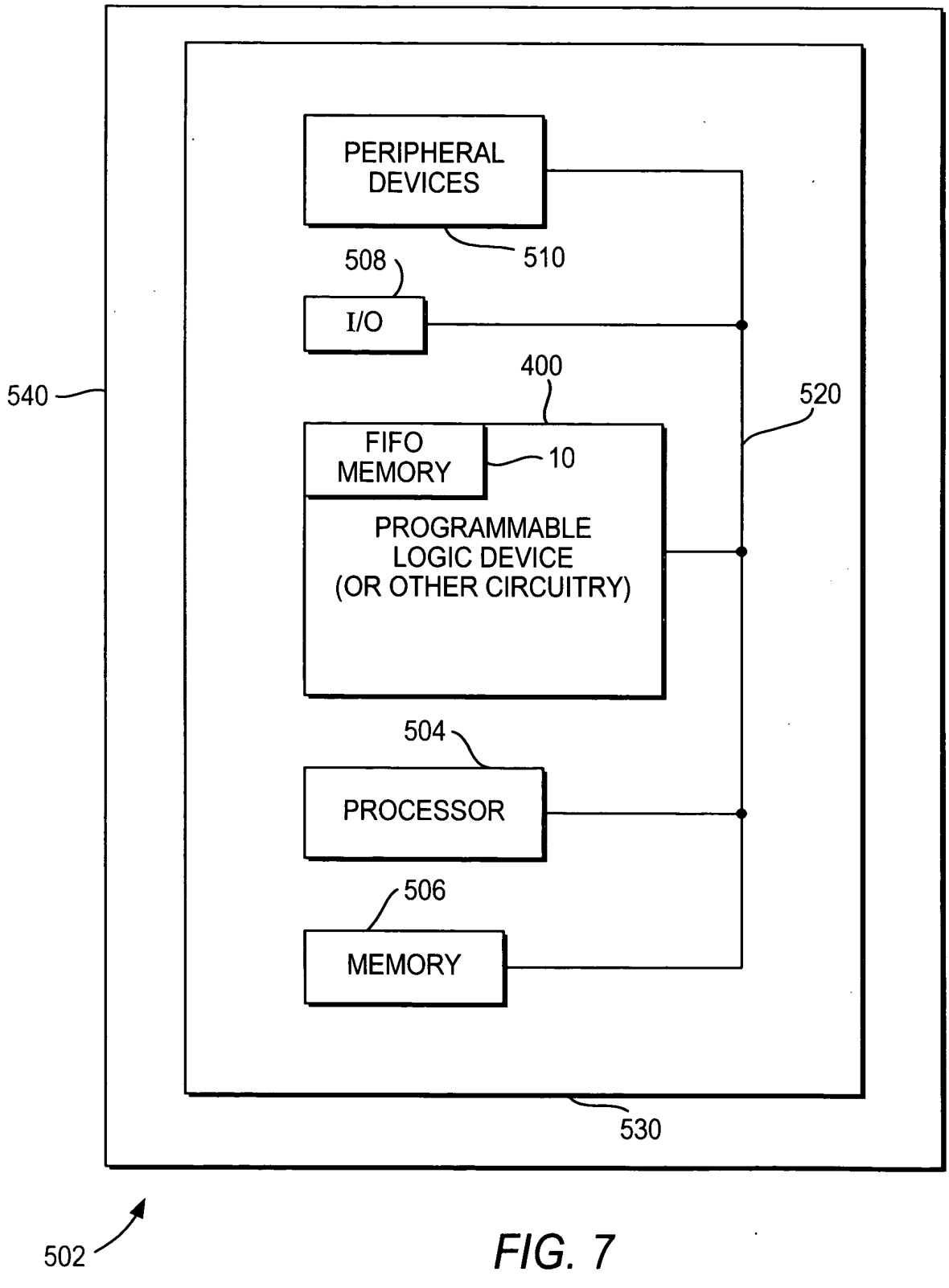

PERIPHERAL DEVICES
510
508
I/O
400
540
520
FIFO MEMORY
10
PROGRAMMABLE LOGIC DEVICE (OR OTHER CIRCUITRY)
504
PROCESSOR
506
MEMORY
530
502

FIG. 7